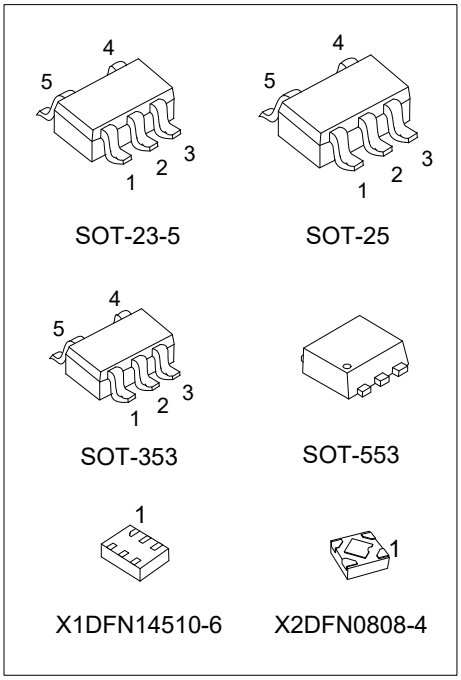
U74LVC1G125

CMOS IC

BUS BUFFER/LINE DRIVER 3-STATE



■ DESCRIPTION

The **U74LVC1G125** is a single bus buffer/line driver with 3-state output. When the output enable ($\overline{OE}$) is high the output will be disabled. In contrast, when the $\overline{OE}$ is low, true data will pass from A input to the Y output.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

■ FEATURES

* Operate From 1.65V to 5.5V
* Inputs Accept Voltages to 5.5V
* High Noise Immunity
* Low Power Dissipation
* Green & Pb Free

■ ORDERING INFORMATION

Ordering Number	Package	Packing
U74LVC1G125G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G125G-AF5-R	SOT-25	Tape Reel
U74LVC1G125G-AL5-R	SOT-353	Tape Reel
U74LVC1G125G-AN5-R	SOT-553	Tape Reel
U74LVC1G125G-KAP-R	X1DFN14510-6	Tape Reel
U74LVC1G125G-KAR-R	X2DFN0808-4	Tape Reel

U74LVC1G125G-AE5-R
(1)Packing Type
(2)Package Type
(3)Green Package

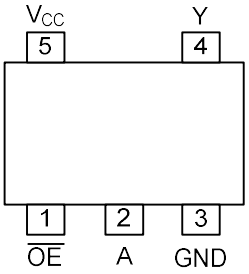
(1) R: Tape Reel
(2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353
AN5: SOT-553, KAP: X1DFN14510-6
KAR: X2DFN0808-4
(3) G: Halogen Free and Lead Free

■ MARKING

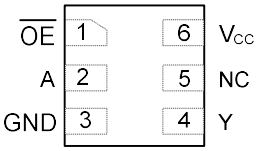
SOT-23-5 / SOT-25 / SOT-353 / SOT-553	X1DFN14510-6 / X2DFN0808-4
5 4 3L5G 1 2 3	3U

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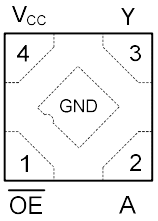
■ PIN CONFIGURATION



SOT-23-5 / SOT-25
SOT-353 / SOT-553



X1DFN14510-6
(TOP VIEW)



X2DFN0808-4
(TOP VIEW)

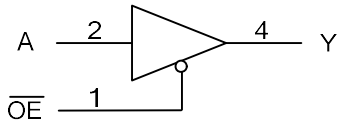
■ FUNCTION TABLE

INPUT($\overline{OE}$)	INPUT(A)	OUTPUT(Y)
L	L	L
L	H	H
H	X	Z

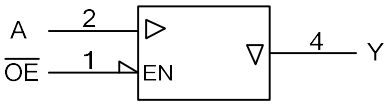
Note: H: HIGH voltage level; L: LOW voltage level; X=don't care; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (Positive Logic)

For SOT-23-5/SOT-25/SOT-353/SOT-553/X1DFN14510-6

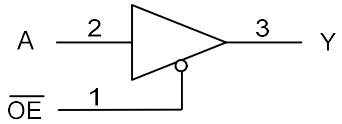


Logic Symbol

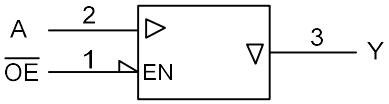


IEC Logic Symbol

For X2DFN0808-4



Logic Symbol



IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified) (Note 1、3)

PARAMETER		SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage		V_{CC}		-0.5 ~ +6.5	V
Input Voltage (Note 2)		V_{IN}		-0.5 ~ +6.5	V
Output Voltage (Note 2)	Enable mode	V_{OUT}		-0.5 ~ V_{CC} + 0.5	V
	Disable mode			-0.5 ~ +6.5	V
	Power-down mode			-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}		±100	mA
Continuous Output Current		I_{OUT}	V_{OUT}=0 to V_{CC}	±50	mA
Input Clamp Current		I_{IK}	V_{IN}<0	-50	mA
Output Clamp Current		I_{OK}	V_{OUT}<0	-50	mA
Power Dissipation	SOT-23-5	P_D	T_A=-40°C ~ +125°C	300	mW
	SOT-25			360	mW
	SOT-353/SOT-553			250	mW
	X1DFN14510-6			200	mW
	X2DFN0808-4			250	mW
Storage Temperature		T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. It's guarantee by design, this parameter is not production tested.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-23-5	θ_{JA}	280	°C/W
	SOT-25		230	°C/W
	SOT-353		350	°C/W
	SOT-553		370	°C/W
	X1DFN14510-6		440	°C/W
	X2DFN0808-4		350	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	V_{CC}=1.65V ~ 5.5V, Enable mode	0		V_{CC}	V
		V_{CC}=1.65V ~ 5.5V, Disable mode	0		5.5	V
		V_{CC}=0V, Power-down mode	0		5.5	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta V$	V_{CC}=1.65V ~ 2.7V			20	ns/V
		V_{CC}=2.7V ~ 5.5V			10	ns/V
Operating Temperature	T_A		-40		+125	°C

Note: It's guarantee by design, this parameter is not production tested.

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V ~ 1.95V	0.65×V_{CC}			0.65×V_{CC}			V
		V_{CC}=2.3V ~ 2.7V	1.7			1.7			V
		V_{CC}=2.7V ~ 3.6V	2			2			V
		V_{CC}=4.5V ~ 5.5V	0.7×V_{CC}			0.7×V_{CC}			V
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V ~ 1.95V			0.35×V_{CC}			0.35×V_{CC}	V
		V_{CC}=2.3V ~ 2.7V			0.7			0.7	V
		V_{CC}=2.7V ~ 3.6V			0.8			0.8	V
		V_{CC}=4.5V ~ 5.5V			0.3×V_{CC}			0.3×V_{CC}	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 5.5V, I_{OH}=-100μA	V_{CC} -0.1			V_{CC} -0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			0.95			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			1.7			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			1.9			V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3			2			V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			3.4			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA			0.1			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45			0.7	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3			0.45	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4			0.6	V
		V_{CC}=3.0V, I_{OL}=24mA			0.55			0.8	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55			0.8	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=5.5V or GND			±5			±5	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V			±10			±10	μA
3-State Output OFF-State Current	I_{OZ}	V_{CC} =5.5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=V_{CC} or GND			±10			±10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			10			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=2.3 ~ 5.5V, V_{IN}=V_{CC} -0.6V, I_{OUT}=0			500			500	μA

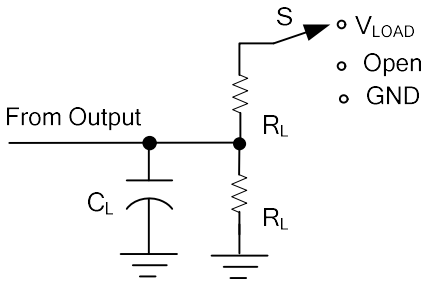
Note: It's guarantee by design, this parameter is not production tested.

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay From Input A to Output Y	t_{PLH} / t_{PHL}	C_L=30pF	V_{CC}=1.8V±0.15V, R_L=1KΩ	1	12	19			21	ns
			V_{CC}=2.5V±0.2V, R_L=500Ω	0.5	10	15			17	ns
		C_L=50pF, R_L=500Ω	V_{CC}=2.7V	0.5	9	12			14	ns
			V_{CC}=3.3V±0.3V	0.5	8	11			12	ns
			V_{CC}=5V±0.5V	0.5	6	9			10	ns
3-State Output Enable Time From Input $\overline{OE}$ to Output Y	t_{PZH} / t_{PZL}	C_L=30pF	V_{CC}=1.8V±0.15V, R_L=1KΩ	1	15	19			21	ns
			V_{CC}=2.5V±0.2V, R_L=500Ω	0.5	12	15			17	ns
		C_L=50pF, R_L=500Ω	V_{CC}=2.7V	0.5	9	12			14	ns
			V_{CC}=3.3V±0.3V	0.5	6	9			11	ns
			V_{CC}=5V±0.5V	0.5	4	7			9	ns
3-State Output Disable Time From Input $\overline{OE}$ to Output Y	t_{PLZ} / t_{PHZ}	C_L=30pF	V_{CC}=1.8V±0.15V, R_L=1KΩ	1	6	10			12	ns
			V_{CC}=2.5V±0.2V, R_L=500Ω	0.5	5	8			10	ns
		C_L=50pF, R_L=500Ω	V_{CC}=2.7V	0.5	4	7			9	ns
			V_{CC}=3.3V±0.3V	0.5	3	6			8	ns
			V_{CC}=5V±0.5V	0.5	3	5			7	ns

Note: It's guarantee by design, this parameter is not production tested.

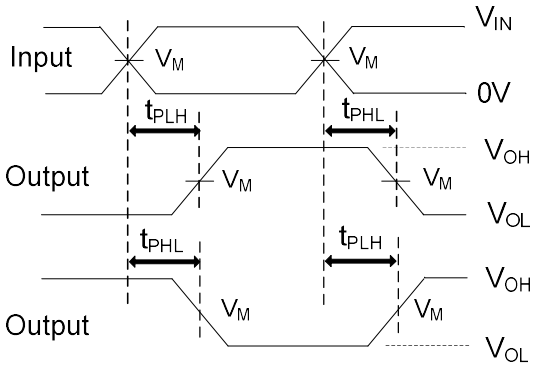
■ TEST CIRCUIT AND WAVEFORMS



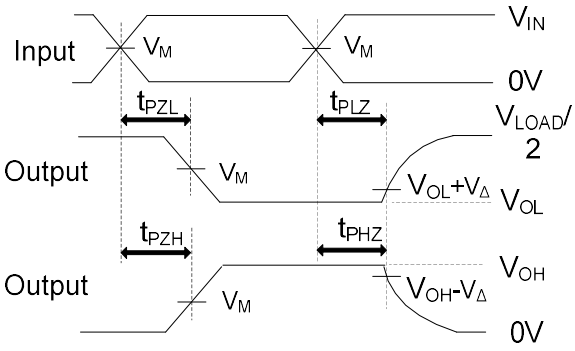
TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	V_Δ	C_L	R_L
	V_{IN}	t_R, t_F					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	0.15V	30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	0.15V	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	0.3V	50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	0.3V	50pF	500Ω



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: P_{RR} ≤ 10MHz, Z_O = 50Ω.

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